REMARKS

Claims 1, 2, 4-22, 33-34, and 36-60 are currently pending. Claims 1, 14, 33, 36, and 55-60 are currently amended to clarify the subject matters as embodied in these claims which Applicants regard as the invention, without acquiescence in the basis for rejection or prejudice to pursue the original claims in a related application. No new matter has been added.

I. Claim Rejections Under 35 U.S.C. §101

Claims 33-34, 36-40, and 41-54 stand rejected under 35 U.S.C. §101 for being directed to non-statutory subject matter.

II. Claim Rejections-35 U.S.C. §103

Claims 1-2. 4-13, 15-19, 21-22, 33-34, 36-45, 47-51, 53-55, 57-58, and 60 stand rejected under 35 U.S.C. §103(a) as unpatentable over Passerone, "*Fast Hardware/Software Co-Simulation for Virtual Prototyping and Trade-Off Analysis*", 1997, Proceedings of Design Automation Conference 1997 (hereinafter Passerone) in view of U.S. Patent No. 6,230,114 issued to Hellestrand (hereinafter Hellestrand) further in view of Zivojnovic, *Compiled HW/SW Co-simulation, 1996* (hereinafter Zivojnovic). Applicants respectfully traverse.

A. Claim 1 recites at least the following limitations which claims x and y also similarly recite:

> generating an optimized **assembler code** for the software program;
> generating an **assembler-level C software simulation model** by
> **translating the assembler code** or **disassembling a binary code**, in which the simulation model is annotated with information related to estimation or determination of the performance comprising execution delay based upon architecture of hardware on which the software program runs;
> (emphasis added.)

Applicants first respectfully submit that Passerone does not disclose at least the above claimed limitations as purported in the Office Action.

(a) Claim 1 explicitly recites the claimed limitations of "generating an optimized assembler code for the software program" and "translating the assembler code into an assembler-level C software simulation model . . . ." In contrast, Passerone starts with a "**high level formal language**" which describes the functionality of each block and how they are connected together; Passerone then translates this "high level formal language" description of the system into an intermediate level. **Sec. 2.1, ¶1**. That is, Passerone starts with a high level formal language model and then generates an intermediate level model. This is not, however, the claimed limitations which "generat[e] an optimized **assembler code** for the software program" and "**generat[e] an assembler-level C software** simulation model by translating the assembler or disassembling a binary code" as Passerone merely generates a high-level formal language model first and then translates it into an intermediate level, and a high-level formal language model is not an assembler code. As such, Passerone does not disclose at least this claimed limitations.

(b) Applicants further respectfully submit that Passerone also fails to disclose the claimed limitation of "generating the assembler code into an assembler-level C software simulation model by ***translating the assembler code*** or ***disassembling a binary code***" of claim 1. Firstly, Passerone is absolutely silent on disassembling any binary codes. Secondly, Passerone only discloses some translation twice in its entirety. Passerone uses POLIS to translate a formal specification of the system into a "network of CFSMs," **Section 2.2**, and into an "intermediate format" for optimization in speed and size, **Section 2.1**. However, Passerone is also silent on translating an assembler code into an assembler-level C software simulation model as claimed in claim 1. Thus, Passerone also fails to disclose the above claimed limitation.

(c) Passerone does not disclose annotating the simulating model with information related to estimation or determination of performance including executing delay. To the contrary, Passerone explicitly states that "[t]he **execution delay** of a CFSM transition is **unknown a priori**. It is **only assumed to be non-zero** . . . ." **Sec. 2, Second Bullet, Subsection 1**. Thus, Passerone not only does not disclose the above claimed limitation but actually admits that the

execution delay can only be assumed to be non-zero. Passerone thus fails, again, to disclose the aforementioned claimed limitations.

B. Applicants respectfully submit that Zivojnovic fails to cure Passerone's deficiency as Zivojnovic is absolutely silent on annotating the simulation model.

Moreover, not only does Zivojnovic fail to cure Passerone's deficiency, Zivojnovic actually teaches away from the claimed invention, and combining Passerone, Hellestrand, and Zivojnovic renders at least Zivojnovic unsatisfactory for its intended purpose.

Zivojnovic discloses a technique for simulating processors and attached hardware using compiled simulation. **Abstract and Sec. I, Introduction**.

On the other hand, Hellestrand explicitly discloses that "the Image_TX module 831 is ***a user program in 'C' code*** running on an embedded system . . . ." **Col. 12, ll. 37-39** (emphasis added.) That is, at least the Image_TX module is in C code in Hellestrand. Similarly, Passerone also indicates that "each S-graph node corresponds roughly to a basic block of code, that is a single-input, single-output sequence of ***C code statements***." **Sec. 2.1**, right-hand column, and "[t]he formal specification . . . is . . . synthesized as ***timing-annotated C code*** . . . ." **Sec. 2.2**, ¶1 (emphasis added). That is, part of Passerone's code is also in C code.

Nonetheless, Zivojnovic explicitly states that "[i]f the same algorithm is expressed in C, and compiled using the C compiler . . . the resulting code . . . on the simulator would last for 2 days and 3 hours. Obviously, ***any experimentation with application-oriented compiler and processor adaptions is impossible***." **Sec. II**, second full paragraph on the right-hand column (emphasis added.)

Therefore, combining Passerone, Hellestrand, and Zivojnovic renders at least Zivojnovic unsatisfactory for its intended purpose as Passerone and Hellestrand explicitly call for the use of C code which is expressly disclaimed by Zivojnovic. As such, Zivojnovic cannot be combined with Passerone and Hellestrand to preclude the patentability of the pending claims for the purpose of 35 U.S.C. §103(a).

As such, Applicants respectfully submit that the currently pending claims are believed to be allowable over Passerone, Hellestrand, and Zivojnovic for at least the foregoing reasons.

C. Claim 55 recites the following limitations:

> associating performance information comprising an ***predicted execution delay with an element of the assembly language*** software module; and
> (emphasis added.)

The Office Action purports that Passerone discloses the above claimed limitations of claim 55. Applicants respectfully disagree.

To the contrary, Passerone explicitly states that "[t]he **execution delay** of a CFSM transition is **unknown a priori**. It is **only assumed to be non-zero** . . . ." **Sec. 2, Second Bullet, Subsection 1**. Thus, Passerone not only does not disclose the above claimed limitation but actually admits that the execution delay can only be assumed to be non-zero. Passerone thus may not incorporate predicted execution delay. Therefore, Passerone fails to disclose the aforementioned claimed limitations. As such, Applicants respectfully submit that claim 55 and its respective dependent claims are believed to be allowable over the cited prior art references.

III. Claim Rejections-35 U.S.C. §103(a)

Claims 14 and 46 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Passerone as modified by Hellestrand and Zivojnovic further in view of Hartoog et al, *Generation of Software Tools from Processor Descriptions for Hardware / Software Codesign*, Proceedings of the 34th Design Automation Conference, June 9-13, 1997 (hereinafter Hartoog.) Applicants respectfully traverse.

Applicants respectfully submit that since Passerone, Hellestrand, and Zivojnovic fail to disclose all the claimed limitations of the base claims from which claims 14 and 46 disclose, claims 14 and 46 are thus also believed to be allowable over Passerone, Hellestrand, Zivojnovic, and Hartoog, regardless whether or not Hartoog discloses the claimed limitations

of claims 14 and 46. Claim 14 is nonetheless currently amended to better conform its claim language to the base claim from which claim 14 depends.

IV. Claim Rejections-35 U.S.C. §103(a)

Claims 20, 52, and 59 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Passerone as modified by Hellestrand and Zivojnovic further in view of Suzuki et al, *Efficient Software Performance Estimation Methods for Hardware/Software Codesign*, 1996 Proceedings of the 33rd Annual Conference on Design Automation (hereinafter Suzuki.) Applicants respectfully traverse.

Applicants respectfully submit that since Passerone, Hellestrand, and Zivojnovic fail to disclose all the claimed limitations of the base claims from which claims 14 and 46 disclose, claims 20, 52, and 59 are thus also believed to be allowable over Passerone, Hellestrand, Zivojnovic, and Suzuki, regardless whether or not Suzuki discloses the claimed limitations of claims 20, 52, and 59.

CONCLUSION

Based on the foregoing, all claims are believed allowable, and an allowance of the claims is respectfully requested. If the Examiner has any questions or comments, the Examiner is respectfully requested to contact the undersigned at the number listed below.

The Commissioner is authorized to charge any fees due in connection with the filing of this document to Bingham McCutchen's Deposit Account No. **50-4047**, referencing billing number **7012162001**. The Commissioner is authorized to credit any overpayment or to charge any underpayment to Bingham McCutchen's Deposit Account No. **50-4047**, referencing billing number **7012162001**.

Respectfully submitted,
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